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Data Collection Function of Ferroelectric Memory in Intelligent High-speed Vehicle Monitoring System

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Abstract: With the rapid development of information science and technology, the application of high-speed data acquisition and storage systems has become more and more extensive, and the development of China's highways also provides a good opportunity for high-speed data acquisition. At the same time, along with the improvement of manufacturing technology and manufacturing capacity, the speed and capacity of collection have been improved to varying degrees. However, due to a late start in China, the development is relatively backward. Therefore, the research on a high-performance data collection and storage system is Very necessary. This article aims to study the development and design of a monitoring system for high-speed vehicles. To this end, this paper proposes a method for the data acquisition function of ferroelectric memory, which improves the monitoring capability of the high-speed vehicle monitoring system through the selection of the large-capacity storage capacity of the ferroelectric memory and the selection of the data acquisition method. Simultaneously, a simulation experiment is designed to analyze and compare the data collection and storage function of the system. The experimental results in this article show that the improved system has a 95% increase in data collection and storage capacity compared with the previous method. The nearly 2 times increase can effectively improve China's The ability to monitor high-speed vehicles.

1. Introduction

With the gradual development of scientific research and other related technologies, more and more people need to face the problem of multiple signal processing, and the process of multiple signal processing has very high requirements for data acquisition and storage capacity of the storage system. . We need to know that the core technology of the information age is the pursuit of information technology, and information collection, processing, and preservation are the core of information technology, that is, the core of the core, and its importance is self-evident. Therefore, it is very necessary for high-performance information collection and information storage. At present, the application fields of data acquisition and storage systems are relatively extensive. The research on this important subject in the field of data acquisition requires continuous development and exploration.

The difference is that the key to data collection technology, foreign countries are quite mature and attach importance to the research and development of its technology. The number of channels is different, and the ability to collect information is also very different. There are mainly the following different division methods, namely single, dual and multi-channel three methods are more common, and the sampling rate is also quite different, up to Ghz Down to kHz, the resolution is also divided from 8-bit resolution to 16-bit resolution. However, in the early years, China did not pay enough attention to related fields. As a result, China's development started relatively late. Most of the technology accumulation was not enough, and the maturity of technology was not enough to support us to carry out related research. But now, as a large number of companies and research institutions have higher and higher requirements for related performance, China has invested more and more in related research. This is an excellent opportunity for us to experiment with overtaking on a curve.

In recent years, the main research directions of high-speed data acquisition and data storage systems at home and abroad have focused on the research of data storage and data acquisition in related fields. Ferroelectric storage has excellent performance and fast storage speed. The large storage capacity and other characteristics have made more and more people begin to invest in his research. Thuau D believes that studying the mechanical strain of the electrical characteristics of ferroelectric OFET base memories is essential for new flexible printed circuits. In this regard, he studied the effects of compressive and tensile strains applied parallel, 45° angle and perpendicular to the semiconductor channel, indicating the key factors that need to be considered before designing a flexible memory [1]. Jung SW uses a rigid polyimide island structure to fabricate a stretchable organic ferroelectric memory transistor (OFMT) on a polydimethylsiloxane substrate. In addition, his memory TFT exhibits excellent mechanical stability, with no significant changes in electrical performance under large strains of up to 50%. These results show the feasibility of a promising device for stretchable electronic systems [2]. The discovery of Y Li's HfO2-based ferroelectric (FE) film provides FE storage devices with next-generation storage technology. He proposed that TiNx with different nitrogen atom content proved to be the electrode of FE Hf0.5Zr0.5O2 memory device on quartz substrate for transparent memory applications. The polarization cycle performance of FE TiNx/Hf0.5Zr0.5O2/TiNx has been explored up to 107 times. Devices with nitrogen-rich TiNx electrodes exhibited suppression of wake-up effects during cycling [3]. A, Saeidi first proposed and theoretically tested the implementation and operation of a silicon-doped HfO2 non-volatile ferroelectric memory (NVM) tunnel field effect transistor, indicating that the ferroelectric non-volatile tunnel field effect transistor (Fe-TFET) can be used as Ultra-low voltage operation can power non-volatile memory even in aggressively scaled sizes. The theoretical results provide unique insights into how the device geometry and ferroelectric properties affect the transfer characteristics of Fe-TFETs [4]. Madsen EK proposed that when working with individuals with intellectual and developmental disabilities (IDD), it is often necessary for direct caregivers to collect personal behavioral data, which is used as the basis for the implementation of experience-based interventions and treatments. Due to limited resources, indirect and descriptive measures of challenge behavior are used to analyze the functions of individual behaviors, rather than the preferred multimodal evaluation method, which includes experimental function analysis. In order to ensure that IDD individuals are provided with the most effective services and support, accurate and consistent data collection is essential [5]. Medley-Rath believes that the popularity of Facebook (FB) has prompted researchers to seek ways to use social media platforms in empirical research. One way is to use FB's secret group tool for asynchronous online focus groups. In the research report, he outlined the steps to use the FB secret group and the advantages and disadvantages of this method. Three asynchronous online focus groups were conducted using the secret group function of FB. I recruited caregivers of children with sensory processing disorders or "feeling problems", and they participated by writing their experiences online [6]. Bragana S proposed that in the past, anthropometry used traditional measurement techniques to record the size of the human body. Nowadays, human body size research can be carried out more effectively using 3D body scanners, which can provide a large amount of body measurement data faster than traditional techniques. He introduced a wide range of issues related to the use of 3D body scanners to collect anthropometric data, including the different types of technologies available and their impact, standard scanning procedures required for effective data collection, and possible sources that may affect the reliability of the collected data And the measurement error of validity [7]. Zhong P believes that in the wireless rechargeable sensor network (WRSN), there is a way to use mobile vehicles to charge nodes and collect data. These two types of vehicles, data collection vehicles (DCV) and wireless charging vehicles (WCV), are used to achieve high efficiency in data collection and energy consumption. In addition, they designed an optimization function to achieve the maximum data throughput by adjusting the data rate and link rate of each node [8]. The above-mentioned documents describe the ferroelectric memory and data collection functions quite well, and have made great efforts to support the related theory. However, many researches are still in the theoretical stage, and they have not verified their theories through the design experiment area. As a result, the experimental technical support for many research topics is not enough, and it is difficult to support the correctness of their own theories.

The innovation of this paper is to take the design of the data acquisition system as the technical support, the model design of the ferroelectric memory and the optimization of its storage method as the innovation, and the theoretical support of the performance analysis of the ferroelectric memory, through the design of the high-speed vehicle monitoring system and Research on the composition of the modules and design the most efficient data collection and storage system, which greatly improves the overall collection efficiency and accuracy.

2. Monitoring System Related Methods

2.1. Data Acquisition System

The data acquisition system combines data acquisition control, industrial bus communication and wireless communication. The whole system is divided into data acquisition terminal, control display terminal, transmission communication terminal, and website server [9]. A brief model of the system is shown in Figure 1.

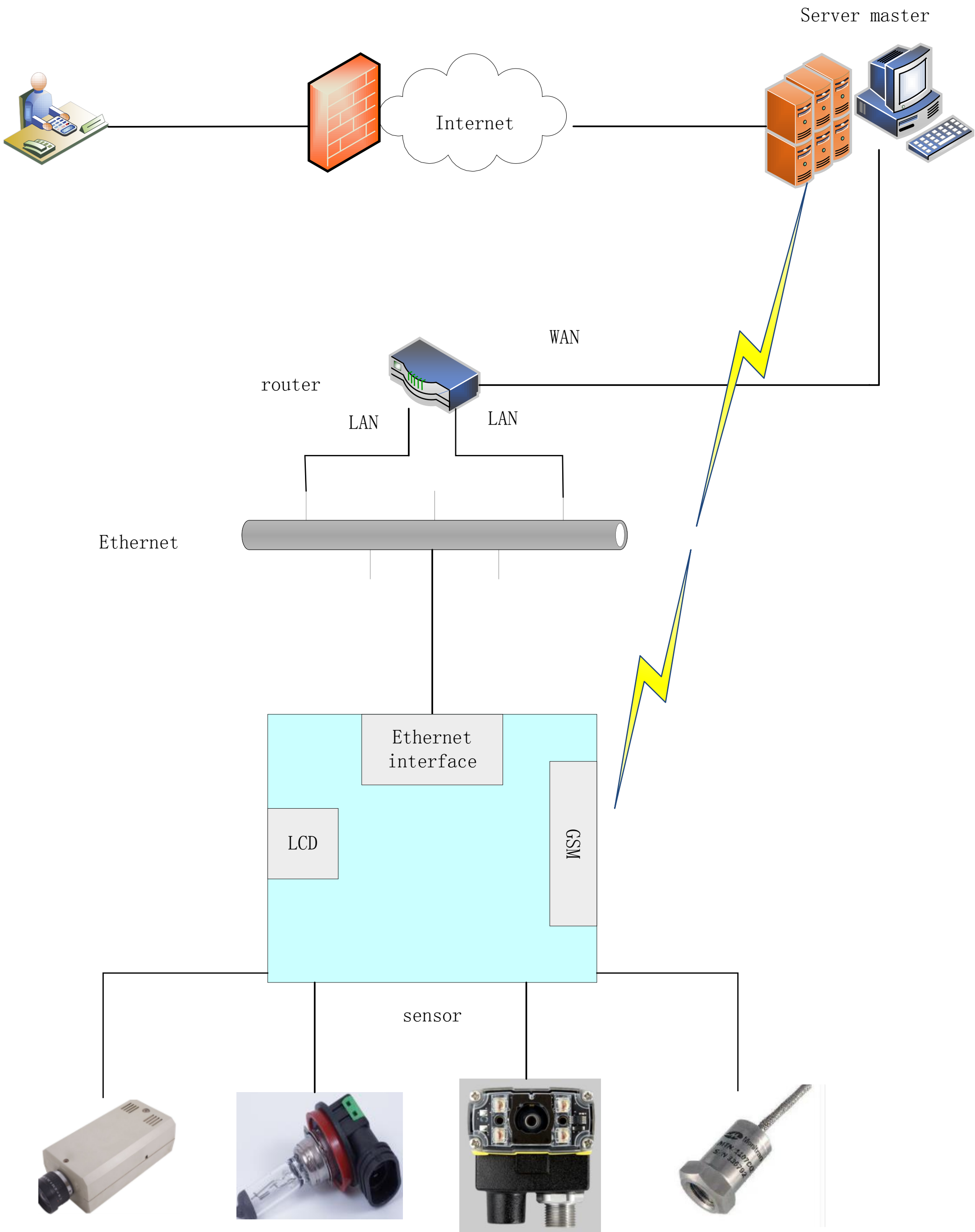

Figure 1. Data acquisition system model

(1) Data collection terminal

The data acquisition terminal completes the system's acquisition of digital and analog signals, and transmits the conditioned digital and analog signals to the MCU for centralized processing. The data acquisition terminal can complete 16 channels of 0-12V voltage acquisition or 16 channels of 0-20mA current acquisition [10].

(2) Control the display terminal

The control display terminal is composed of a main control chip and an LCD touch screen. For the realization of its comprehensive scheme and system cost, the main control chip is STMicroelectronics' STM32F103VE based on the armcortex-m3 core.

(3) Transmission communication terminal

In order to facilitate the timely transmission of control and data, the data acquisition system supports a variety of transmission communication methods, including: Ethernet network communication, GSM wireless communication, CAN/RS-485/232 communication.

(4) Web server side

The collected data is uploaded to the Web site server, and the data can be queried through the Internet [11].

GSM/GPRS wireless communication is flexible and convenient to use, Ethernet wired communication is stable, and the network speed is fast. In order to meet the different needs of users, this system uses these two communication methods at the same time. Therefore, GSM and Ethernet technologies have become the key technologies of the system. The composition structure of its communication system is shown in Figure 2:

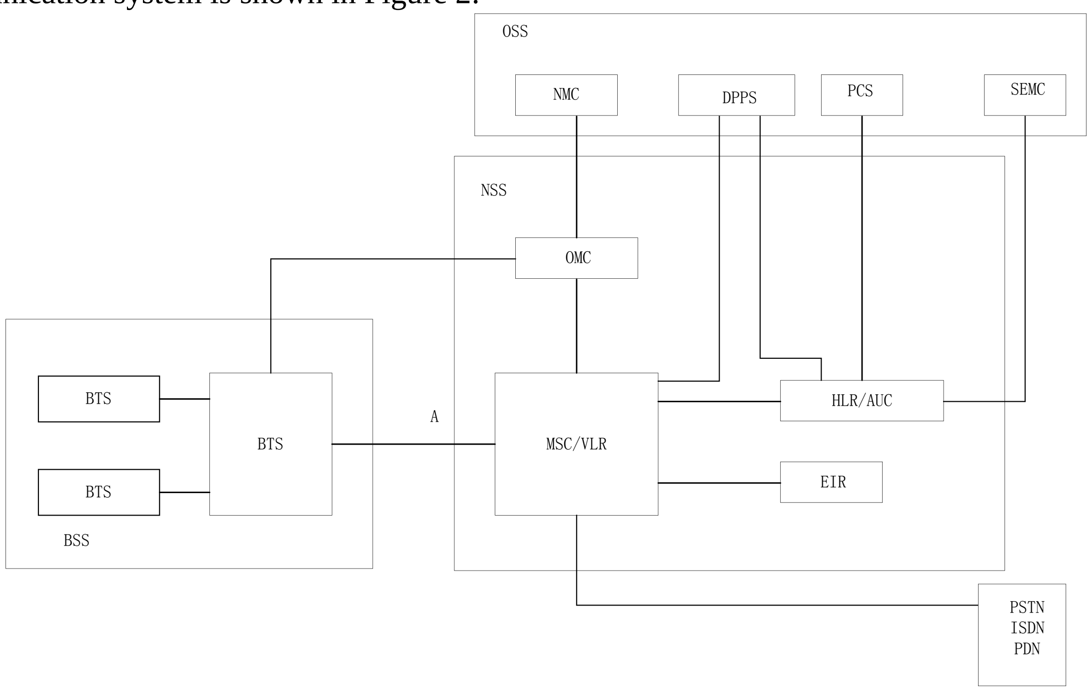

Figure 2. Composition and structure of the communication system

(5) Overall hardware design

The system hardware framework is shown in Figure 3. The system uses the ARM Cortex-M3 core as the main control chip, which is mainly equipped with collection and adjustment modules, display touch modules and other corresponding peripheral devices and circuits to complete data collection, display and sending functions, Industrial bus module, power supply module, GSM wireless transmission module, Ethernet transmission module[12].

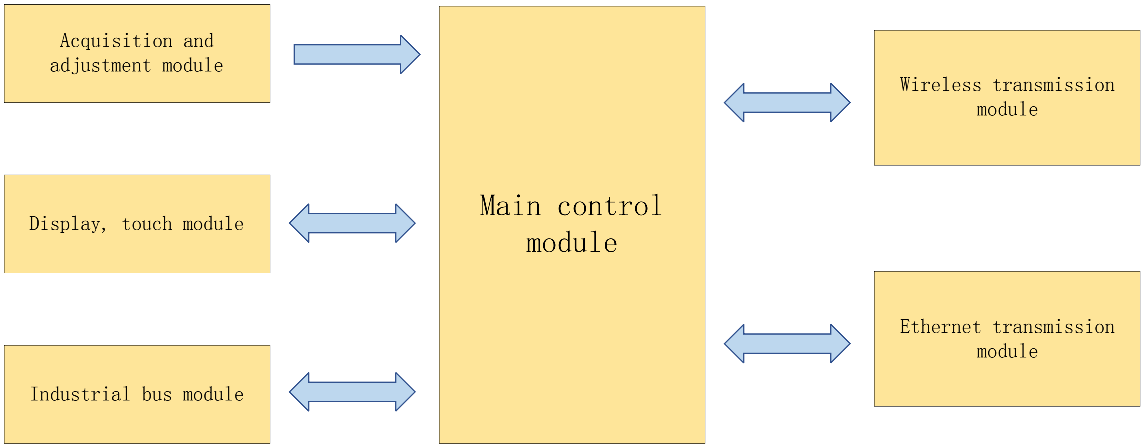

Figure 3. Overall structure of the hardware

2.2. Ferroelectric Capacitor Model

The ferroelectric capacitor model of Ramtron, a major manufacturer of ferroelectric memory products, is a ferroelectric capacitor transient model, which is an improved Miller model, which has been embedded in the circuit simulation software HSIM and the device simulation software Silvaco software .

This model is based on the following assumptions: 1. The hysteresis loop is symmetric with respect to the origin. Two: The electric hysteresis loop has nothing to do with frequency. In addition, other nonlinear effects, such as ferroelectric fatigue and imprinting effects, are not considered in the model [13].

The model uses a mathematical function to describe the PV relationship, thereby simplifying modeling and improving circuit simulation speed, but the specific parameters in the model have no clear physical meaning, so this model is only suitable for circuit simulation and cannot be used for ferroelectric thin films Development. The normalization equation is as follows:

$$F_{LK}(V) = \frac{P_K(V)-P_k(-V_{PK})}{P_K(V_{PK})-P_k(-V_{PK})} \quad (1)$$

For the function$F_{LK}(V)$, there is a minimum value of 0 when $V = -V_{PK}$, and a maximum value of 1 when $V = V_{PK}$. Its differential form is:

$$f_{LK} = \frac{dF_{LK}(V)}{dV} \quad (2)$$

Therefore, the polarization change ΔP when the voltage changes from V to V+ΔV is:

$$\Delta P = \left(P_K(V_{PK}) - P_K(-V_{PK})\right) f_{LK}(V)\Delta V \quad (3)$$

Because it is assumed that the electric hysteresis loop is symmetrical with respect to the origin, the high half-branch curve is an image in which the lower half-branch curve is symmetrical with respect to the origin in the P-V plane. So its polarization change is:

$$\Delta P = P_x f_{LK}(V)\Delta V \tag{4}$$

Here, P_x can be expressed as follows according to the symmetry of the electric hysteresis loop:

$$P_x = 2P_m/F_{LK}(V_m) - F_{LK}(-V_M) \tag{5}$$

Among them $(V_m,\ P_m)$ is the end point of the electric hysteresis loop.

In this model of HSIM, a second-order fractional equation is used to curve-fit the probability density function $F_{LK}(V)$, and the probability density function $F_{LK}(V)$ uses the following form:

$$f(x) = \frac{a_1}{1+(b_1(x-c_1))^2} + \frac{a_2}{1+(b_2(x-c_2))^2} \tag{6}$$

The integral form of Equation 6 is:

$$F(x) = d0 + \left(\frac{a_1}{b_1}\right) tan^{-1}\big(b_1(x-c_1)\big) + \left(\frac{a_1}{b_1}\right) tan^{-1}\big(b_2(x-c_2)\big) \tag{7}$$

The temperature coefficient of each parameter is obtained by fitting the temperature influence of the above parameters and stored in the temperature parameter file. This model can be used to simulate the P-V hysteresis curve, the transformation between the hysteresis loops, the transient response under voltage pulses, and the influence of temperature on the hysteresis loops, etc [14].

2.3. Ferroelectric Memory

The more common mature system is mainly divided into two parts. Among them, the data in the volatile memory will be lost when the system is suddenly powered off, but the RAM will not, and it will be more convenient to use, and the performance will be more convenient. Far surpasses other memory of the same type [15].

Since the ferroelectric memory was developed, it has shown performance advantages that other memories do not have. At the same time, its storage capacity is far more than other similar types of memories. Table 1 shows the comparison of storage performance between ferroelectric memory and other types of memories [16].

Table 1. Performance comparison of several kinds of memories

	Volatile memory		Non-volatile memory	
	DRAM	SRAM	FLASH	FERAM
Number of writes	$>10^{15}$	$>10^{15}$	$10^{5\text{-}6}$	$10^{6\text{-}12}$
Read times	$>10^{15}$	$>10^{15}$	$>10^{15}$	$10^{6\text{-}12}$
Write speed	50ns	10ns	1ns	100ns
Quiescent Current	10A	1A	1A	1A
Relative unit area	1	4	0.8	1

In addition, compared with EEPROM, the following can be found. FRAM has the fastest writing speed, and there is no need to wait for a long time when writing. A few milliseconds can complete the work that others can take a long time to complete [17].

The second major advantage of ferroelectric memory (FRAM) is that there is almost no limit to the number of writes. If EEPROM can only handle writes from 100,000 (10 to the 5th power) to 1 million, the new generation of strong media memory (FRAM) will reach 100 million. At the same time, there is another advantage of ferroelectric memory that others don't have. Its energy consumption is very low. The writing speed of other memories is too slow. This is because it takes a long time to supply power, which leads to relatively low current. Big, consumes a huge amount of energy.

Application of ferroelectric memory:

At the same time, the flash memory speed of ferroelectric memory is very fast, and this feature means that it is very suitable for contactless tolling on highways. Through the integration on the circuit card, the vehicles on the high-speed do not need to manually charge one by one when they pass the toll station. At the same time, the anti-interference ability of the external environment is also relatively strong, and the high-speed has also been effectively eliminated. The influence of noise and various environmental factors [18]. Its main application is shown in Figure 4:

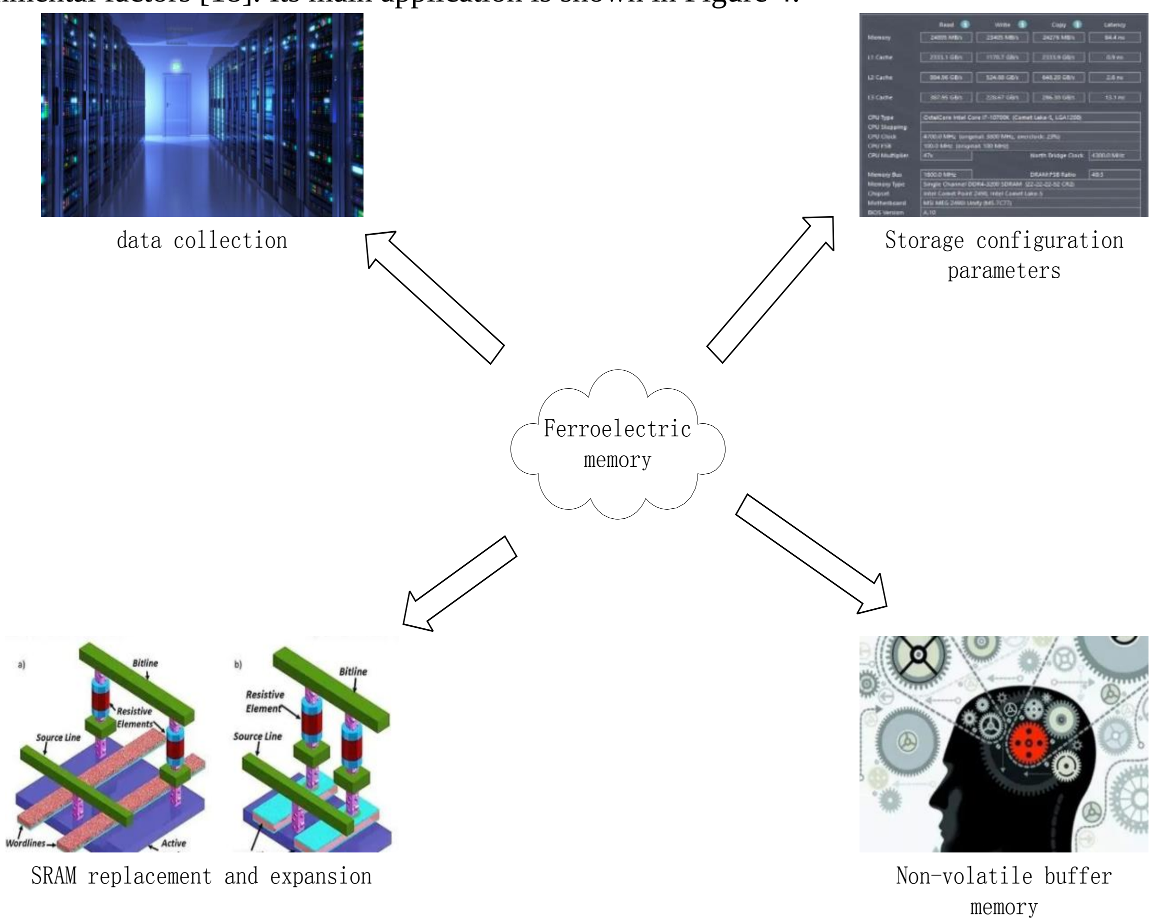

Figure 4. Several major applications of ferroelectric memory

With the rapid development of electronic products, the development of memory has also taken a leap, but the storage capacity and energy consumption of mainstream memory are very poor, and there is an urgent need for a memory with low energy consumption and fast writing speed to replace it. , And ferroelectric memory came into being. As shown in Table 2, the performance comparison of several commonly used memories on the market today [19].

Table 2. Performance comparison of several common memories

Model	Stand-by current	Write current	Number of writes	Write time	Full time
FM24C1	10	150	13	72	47
AT24C1	18	3	6	10	1.3
ST24C1	300	2	6	10	1.3
24AA16	100	3	6	10	1.3
X24C16	150	3	6	10	1.3

Ferroelectric memory is increasingly used in various tool meters, measuring and medical instruments, non-contact smart cards, access control systems, and automotive black boxes. Mass production is now possible, and it can be said that it has entered the era of mass production [20].

3. High-Speed Detection System Data Acquisition Experiment

3.1. Signal Sampling Method

With the progress of digital globalization, digital signal processing is widely used in many fields. As an important interface for digital signal processing, analog-digital converters are developed for high-speed, high-precision, and ultra-wideband. Due to the bandwidth limitation of each process, the conversion rate of the single-chip single-process analog-to-digital converter has almost reached its limit. Therefore, in order to solve the problem of high-speed data collection, new methods are needed. For the above reasons, this article analyzes the theoretical knowledge of signal sampling and proposes a sampling method for system design.

(1) Bandpass signal sampling

The process of changing a signal from an analog signal to a digital signal is called sampling, and its mathematical expression is

$$x(n) = x\_a\ (t)| = x(nT) \tag{8}$$

The Nyquist sampling theorem analyzes signals whose frequencies are distributed at (0, f). If the center frequency is very high and the bandwidth is very narrow, it is called a bandpass signal. Because the center frequency is high, if data is obtained according to Nyquist's sampling theorem, the sampling frequency becomes high, and the system cannot meet the requirements. In the process of sampling theorem analysis, the signal spectrum is spread in the frequency domain through sampling. The sampling rate needs to be designed reasonably to prevent the spectrum from being aliased when the spectrum is expanded. This low-sampling method has the same effect as frequency mixing, and the subsequent sampled signal is passed through a digital low-pass filter to obtain a low-frequency signal.

Assuming that the frequency domain of a signal is limited to (f_1, f_h), if the sampling frequency meets the following requirements:

$$\frac{2f_h}{m} \leq f_s \leq \frac{2f_l}{m-1} \tag{9}$$

In the above formula, m needs to meet the following conditions:

$$1 \leq m \leq m_{max} = int\left[\frac{f_h}{|f_h - f_l|}\right] \tag{10}$$

(2) Time interleaved sampling

Due to the limitation of process bandwidth, the sampling rate of the single-chip single-process analog-to-digital converter (ADC) is close to the limit. In order to solve the problem that the sampling rate of the ADC is not high enough, a time interleaved sampling system composed of multiple ADCs can be used to achieve high-speed sampling.

(3) Compressed sampling

Compressed sampling is also called compressed sensing sampling. It is a new sampling theory that is different from the Nyquist sampling theorem. It analyzes the sparse domain of the input signal and uses a very low sampling rate to analyze the data. Compressive sampling uses a much smaller sampling rate than the Nyquist theorem for data collection, and can take full advantage of the advantages of wireless communication, array signal processing, and imaging systems. The comparison of the three sampling methods is shown in Table 3:

Table 3. Comparison of three sampling methods

	Sampling Rate	Sampling chip
Bandpass sampling	Twice the bandwidth	Monolithic ADC
Time interleaved sampling	Double the highest frequency divided by M	M-chip ADC
Compressed sampling	Double the highest frequency	AIC

3.2. Control Circuit

Since the read and write operations of SRAM are completed in a sequence of processes, in order for SRAM to function correctly and effectively, a control circuit is required. The actual circuit does not directly use the chip selection control terminal, that is, the write control terminal. Instead, it directly controls reading and writing. After the three logics are combined through the control circuit, two signals of reading and writing are generated for control. The truth value table of the following control circuit can be obtained. Here, CSB, WEB, OEB are input terminals, and WE' and OE' are output terminals called internal write permission and internal output permission, respectively, which can be used for direct control. The writing and reading circuits of SRAM are all active at low level. The truth table of the control signal is shown in Table 4:

Table 4. Control signal truth table

CSB	OEB	WEB	WE’	OE’	SRAM state
1	/	/	1	1	maintain
0	/	0	0	1	Write
0	0	1	1	0	Write out
0	1	1	1	1	No read no write

It can be seen from Table 4 that when CSB is 1, that is, when the entire SRAM is selected, regardless of the state of OEB and WEB, SRAM does not work and maintains the original state. Only when CSB is 0, SRAM can work normally. At this time, when WEB is 0, the cell selected by the write circuit open is written, etc., regardless of the state of OEB, WE' is 0. 0, WEB 1, OE' is 0, that is, the read circuit is open and can be read Action, when OEB and WEB are both 1, WE' and OE' both output a state of 1, and when the write output circuit is closed, no read or write operation is performed.

3.3. The Working Mechanism of Ferroelectric Memory in the System

There are two types of memory devices that can be used to store data in practical applications, random access memory RAM (randomacizedssmemory), that is, volatile memory, and non-volatile memory (non-volatile memory). For example, SRAM and DRAM are volatile memories. If the power is cut off during operation, the data will disappear immediately. A backup battery must be provided to keep the data from being lost when power is off. Thanks to its high performance, fast access speed and unlimited read and write operations, RAM is usually used as a temporary data storage and exchange area. EPROM, EEP OM, FLASH, etc. belong to non-volatile storage. Because of the feature that data is not lost when power is off, NVM can usually be used to save configuration parameters, store system operating codes, and save a certain amount of important data. According to the design requirements of this article, the POS data collector itself can still save a certain amount of bill information even when the power supply is cut off or accidentally cut off, so non-volatile memory is needed.

Flash and EEPROM types of non-volatile memory mainly use floating gate technology. After changing the voltage of the floating gate memory cell, the charge can be added or removed to determine the "0" and "1" of the memory cell. "State 1W. However, in floating gate technology, a charge spring needs to be used to generate high voltage. The so-called transmission refers to the need to force current to flow through the gate oxide layer during the erasing operation, so additional erasing is required. The write delay is required, usually 5-10 milliseconds. Not only that, the floating gate memory cell is destroyed due to high write power and frequent write operations, which will limit the number of deletions and saves as a result.

Ferroelectric memory is non-volatile memory, but does not use floating gate technology. The storage crystal is made of "synthetic lead-zirconium-iron (PZT)" material. Under the action of the electric field, the central atom of the iron transistor also moves along the direction of the electric field, and finally stops in a low-energy state. After the reverse electric field is applied, the atoms that were originally in the low-energy state move to other low-energy states again along the direction of the electric field. A number of neutral atoms move in the crystalline unit unit to form a combination, and form a polarized charge under the action of an electric field. When the inversion of the ferroelectric domain under the electric field is high, and the polarization charge formed when there is no inversion becomes low, the ferroelectric domain becomes stronger. Due to the binary stable state of the dielectric material, the dielectric can be used For memory. As shown in Table 5, the comparison between ferroelectric memory and other memories. According to the overall design of this article, frequent erasing and writing operations on NVM' are required, and the erasing and writing operations also require certain real-world financial performance.

Table 5. Features of ferroelectric memory

	FRAM	EEPROM	FLASH	SRAM
Unit cell structure	1T	2T	1T	6T
Write cycle time	157ns	6ms	11us	58ns
Durability	1000000000000	1000000	100000	∞
Write operation current	15mA	5mA	20mA	8mA
Stand-by current	5uA	2uA	100uA	3uA

The FRAM ferroelectric memory is used to complete the power-down storage and frequent erasing and writing of data. But before storing these data to prevent power failure or other accidents from causing damage to it, the system needs a temporary storage area to temporarily store these intercepted data. There are two purposes for this, the first is to facilitate management; the second is also a more important point, to increase the margin of the system, so that the effect achieved is that the compatibility of the system is improved. The temporary storage area is similar to a reservoir, the input end receives a fast data stream, and the output end flows to the processing unit at a speed determined by the system. Therefore, in some applications, without the participation of the data buffer, the system will be tight during operation. At this time, if the program design is not rigorous enough, the system may not be able to respond to certain commands, resulting in data loss.

4. Data Collection Error Analysis

4.1. Parallel Dual-Channel Real-Time Sampling Channel Mismatch Error Analysis

(1) Equivalent sampling

The same sampling is mostly used for periodically repetitive sampling signals. This refers to the process of obtaining and reconstructing signal waveforms through multiple triggers and multiple samples.

In the system design, it is clear that the sampled signal is a series of random pulse-encoded signals, so it is not suitable for equal sampling.

(2) Parallel dual-channel real-time sampling

Real-time sampling means that after the trigger signal arrives, the entire data acquisition process is completed at one time. Because sampling is performed at equal time intervals, the maximum sampling frequency must meet the requirements of the Nyquist sampling theorem. Therefore, the bandwidth of the sampled signal is limited in the real-time sampling system.

In contrast, the sampling rate of a fast-sampling ferroelectric memory storage system is twice the sampling frequency of a single channel, and the cost is greatly reduced. The storage speed of the memory is required to be higher than that of a single channel. The channel time is doubled. The system is actually implemented. The difficulty is further reduced and the cost is further reduced.

(3) Analysis of mismatch error

Whether it is high-speed ADC sampling or high-speed digital oscilloscope field, by using parallel multi-channel instead of sampling technology, the sampling rate of the system increases and cannot meet the high-precision requirements during the rate increase. The effective number of bits is still very low. This is limited by the channel mismatch error sampled by the parallel ADC. In actual applications, errors caused by inconsistencies between channels due to the limitations of the circuit manufacturing process of each channel and the inconsistent performance of each AD device are called channel inconsistent errors. This type of error is caused by the unevenness of time and amplitude, so it is also called uneven error. This is mainly due to the time error t150k caused by the mismatch of the sampling clock phase delay of each channel, the offset error ko caused by the mismatch reference level of the ADC of each channel, and the gain caused by the mismatched gain. Error kg. Therefore, in this article, the error of the improved data acquisition function of the ferroelectric memory in the actual use process is measured and analyzed, as shown in Figure 5.:

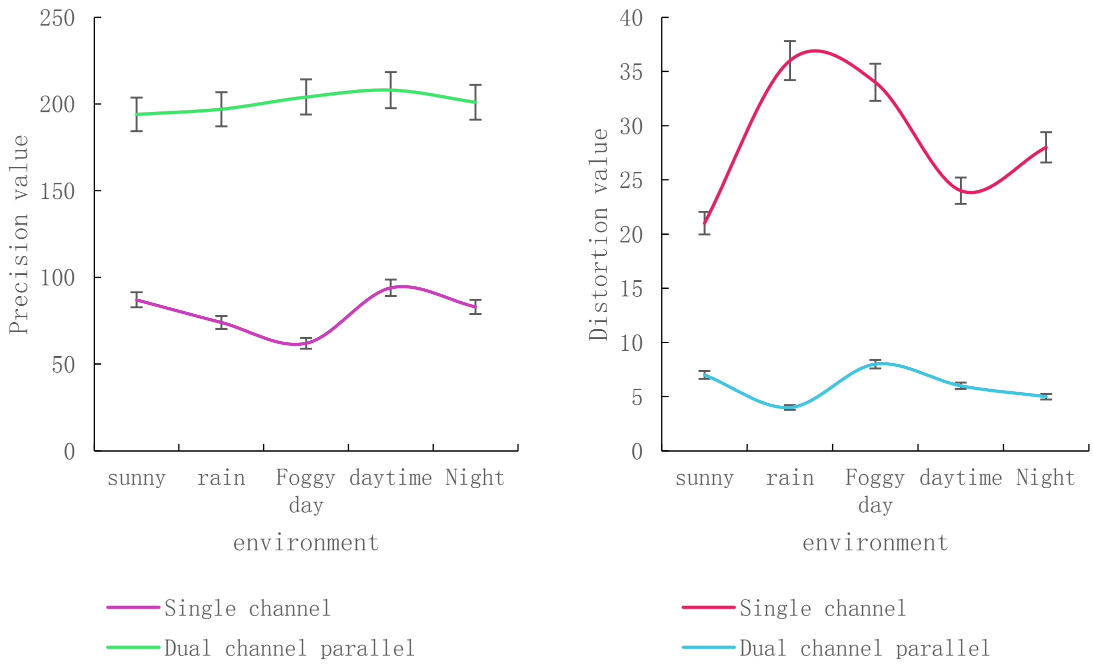

Figure 5. Simulation measurement analysis of accuracy value and distortion value

From the above figure for single-channel and parallel dual-channel measurement of the accuracy value and distortion value, we can see that for traditional single-channel high-speed monitoring data acquisition, it is easy to be affected by different environments, resulting in The detection capability of the system decreases, and the stability of parallel dual-channel detection data collection is relatively high, and the environment has less influence on him. No matter what the environment, the distortion rate of the system is maintained at a stable level. It is not difficult for colleagues to observe its accuracy. It is not difficult to see that the accuracy value of the improved system is more than twice that of the original system, and it has extremely high efficiency.

Regarding the system error problem, this problem has also been considered in the system design, but due to the limited knowledge of this article, the knowledge of error estimation and error analysis is insufficient, the influence of this field can only be controlled to a minimum. Therefore, on the other hand, when designing a printed circuit board, please make the length of the 2-channel clock trace equal. At the same time, the FPGA phase locked loop is used to strictly generate the phase clock. 180°delay of AD conversion.

5. Conclusion

This article mainly studies the intelligent high-speed vehicle monitoring system. Through the research of ferroelectric memory, the optimization and improvement of storage methods and storage paths, and the analogy analysis of several common methods of data collection, the most suitable data is selected. Acquisition method-parallel dual-channel acquisition. Greatly improve the data collection capabilities of the high-speed vehicle monitoring system, and design simulation experiments to analyze the accuracy and distortion rate of data collection. The analysis shows that the improved data collection method has better collection capabilities than the previous collection methods. 95%, which is close to twice the previous rate. While ensuring the efficiency of data collection, it can also ensure the accuracy of collection, which has certain practical application value.

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Data Availability

Data sharing is not applicable to this article as no new data were created or analysed in this study.

Conflict of Interest

The author states that this article has no conflict of interest.

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